Invited - Microfabrication of 3D Terahertz Circuitry

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ABSTRACT — **Advances in micro-fabrication techniques combined with accurate simulation tools has provided the means for the realisation of complex terahertz circuitry. Silicon micro-machining provides the way forward to fabricate accurate rugged structures. Multi-level deep reactive ion etching can be used to replace traditional machining methods achieving smaller feature size, improved surface finish and greater freedom in circuit layout.**
Photonic Bandgap waveguides enable three dimensional arrangements of active devices antennae and filters, and removes the requirement for metallisation of adjoining surfaces. This paper describes some of the state of the art terahertz circuit design and realisation using these techniques.

I. INTRODUCTION

One of the major limiting factors in the advancement of terahertz electronics has been the realization of cheap high performance RF circuitry. Precision conventional machining techniques have been required to manufacture the waveguide cavities which remain the preferred circuit architecture. Thick resist processing has been used to replace conventionally machined components. In particular SU-8 negative resist system can provide accurate waveguide structures but its material properties are not ideal for cooled operation or assembly using solder re-flow techniques. Depths of 1mm are possible but difficult to consistently achieve over the full 100mm wafer diameter.

Anisotropic and isotropic wet etching of silicon can be used to create simple waveguide structures but the limitations resulting from the crystal planes available restrict the circuit dimensions and layout.

Recent advances in Deep Reactive Ion Etching (RIE) technology provide the means to manufacture accurate cavities that are no longer restricted to particular crystal orientations. Depths of 1mm are readily achieved and lithography can be used to give the multi-level structures required for harmonic devices such as subharmonic mixers and frequency multipliers. Using deep RIE techniques a greater level of circuit complexity can be envisaged such that complicated systems such as imaging arrays and power combiners can now be designed and laid out. Accurate 3D simulation tools compliment the technology providing means by which the lithographic processing can refined without the need to prototype and test.

II. TECHNOLOGY

Early attempts at micromachining terahertz waveguide structures utilized thick resist exposure[1]. Combining thick resists such as SU-8 with anisotropic etching of silicon can produce the structures required for waveguide circuits at 500GHz and above. The restrictions for lower frequency operation were mainly in achieving the greater heights required (1mm or more). Recently an ESA funded project StarTiger was able to extend this technology down to 250GHz. StarTiger's main challenge was to design and build a two colour THz imaging array. This was to be used to obtain a passive image a human hand. The frequencies set were 250GHz and 300GHz. With the absence of other detection methods an array of subharmonic mixers was chosen. Two linear arrays of 8 mixers were required to capture the image in more or less real time. As each mixer required its own local oscillator and IF output the design of the full array was challenging.

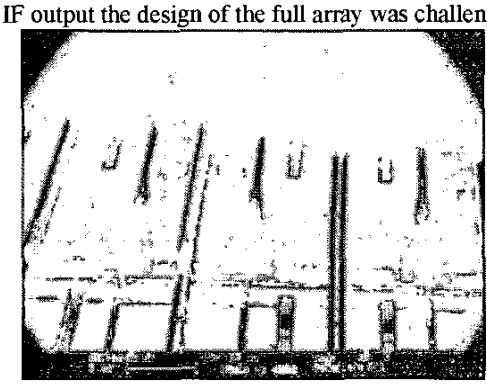

Figure 1: 250GHz subharmonic SU-8 mixer cavity

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This particularly true for micromachined circuitry as no movable tuners can be incorporated as is the case in conventional designs. Therefore Ansoft HFSS was used in conjunction with Ansoft Serenade to model the complete mixer circuit including local oscillator power splitter and feedhorn array. Initially the use of SU-8 and the anisotropic etching of silicon was used. An example of this approach is shown in Figure 1. In order to achieve the dimensions required it was necessary to make use of a combination of mechanical lapping and deep structure UV lithography. The poor thermal match between SU-8 and silicon would not allow the heating or cooling of the finished cavities. Finally, poor adhesion between the SU-8 and the gold metalization resulted in higher losses than predicted. To circumvent these and other problems deep RIE of silicon was adopted.

The complete design of the array required some novel circuit developments. A schematic of the final configuration is shown in Figure 2.

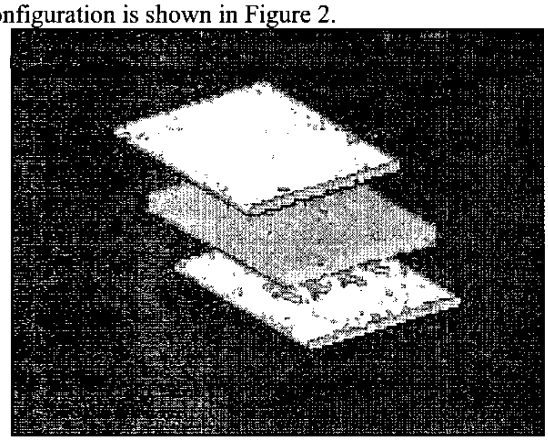

Figure 2: Schematic of the StarTiger Twin Array

The processing required numerous steps however the dimensions associated with the circuit are ideal for deep silicon etching. The central wafer required patterning both sides of a 2.5mm wafer. The thickness of the wafer is guaranteed to a few microns by the vendor Virginia Semiconductor[2]. This is important as this dimension forms part of the optics design setting the separation between the antenna array which is machined conventionally.

A fabricated middle wafer is shown in Figure 3. The processing required numerous processing steps however each is relatively straightforward. Lateral dimensions can be held to better than 5 microns but careful calibration is required to achieve similar control over the depth of critical features. This is particularly true for the thick wafers required for the StarTiger configuration. Etching rates are dependent on the temperature of the active surface. In the etching system used for the project STS[3] the wafer is cooled from the backside, as the wafer is thinned the thermal resistance decreases effecting the etch rate. Careful calibration can minimize this effect.

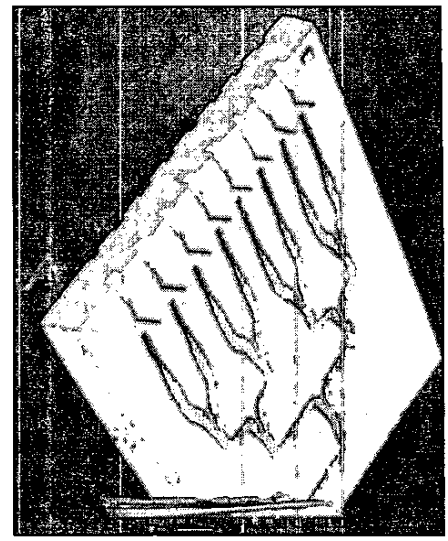

Figure 3: Fabricated centre wafer of the silicon array

The waveguide structures realized had excellent surface finish and mechanical properties. A close up image of the mixer circuit is shown in Figure 4. Once etched the 100mm wafers were cleaned diced and then finally coated in gold to a thickness of two microns.

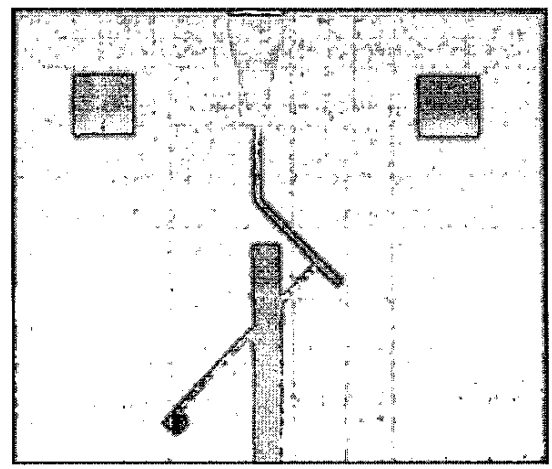

Figure 4: Subharmonic mixer cavity etched in silicon

Much interest has been generated in the application of silicon machined Photonic Bandgap (PBG) material. PBG can be used to suppress unwanted substrate modes for planar circuits. By introducing defects into the crystal lattice, it has been shown that waveguide structures can be realised. The use of deep RIE making use of double sided processing can be used to manufacture layer by layer three

dimensional lattices which incorporate the basic circuit elements of waveguide, bends, power splitters and antenna. Transitions from conventional waveguide and microstrip transmission line enable coupling to the PBG domain thus providing the designer access to the best attributes of either system. PBG circuitry has a major advantage over conventional waveguide that there is no requirement for metalisation reducing ohmic loss.

It is possible to design simple structures in PBG analytically but for complicated waveguide structures it is necessary to use full field simulation. Only recently with emergence of the 64 bit solver from Ansoft has this become possible. In principle the solver is able to tackle very large problems but computing time and available hardware limited the size of models to 7.5Gbyte of RAM. A Sun Systems twin 900MHz processor was used to carry out the calculations. Together these components were able to complete the intense simulations required.

The first task in realising a practical PBG waveguide architecture was to derive a suitable launch from conventional waveguide, this is required in order that the PBG waveguide can be tested. Whilst other PBG structures were considered the basic woodpile structure was adopted largely because its simple geometry permitted the large models to be solved faster and for their ease of manufacturability. A mixture of analytical modelling and empirical optimization was used to find the best configuration. A field plot of this structure is shown in Figure 5

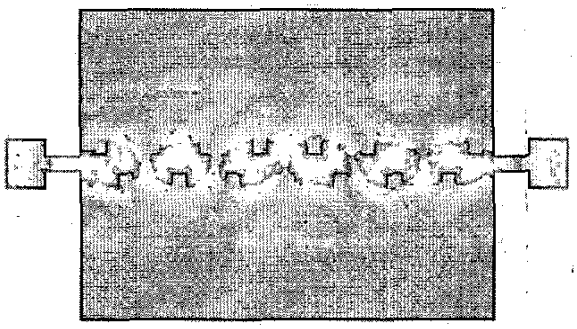

Figure 5: Field plot of the PBG waveguide structure

The predicted return loss for the complete structure is better than 20dB over a 6GHz band within the bandgap.

A mask set was designed which allowed the fabrication of the 250GHz PBG waveguide via deep RIE etching. Holes and pegs were incorporated in the layers to allow them to be assembled in the same manner as childrens construction bricks. The fabrication of the PBG layers was relatively straight forward and the smooth surfaces left by the etching process resulted in a surprisingly robust structure. Previous woopiles fabricated using mechanical machining were more prone to breakage due to the chipping weakening the silicon bars[4].

End plates again etched in silicon and coated in gold were used to perform three functions. These provided the matching from standard height waveguide to the PBG waveguide, confined the field within the crystal and finally provided alignment to the conventional waveguide test fixtures that were necessary in order to test the PBG waveguide at these frequencies. An electron microscope image of the fully assembled PBG waveguide is shown in Figure 6.

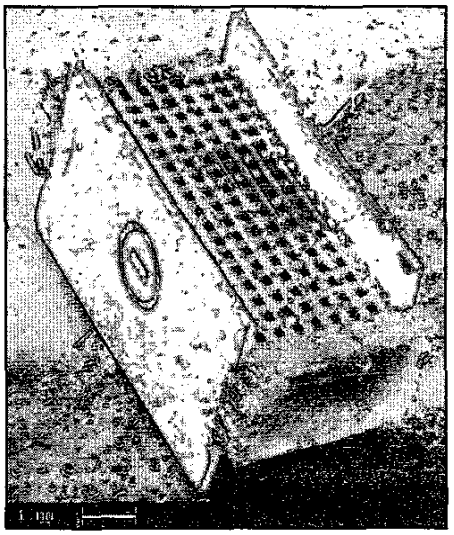

Figure 6: Fully assembled silicon machined PBG waveguide

The use of deep RIE etched silicon for the fabrication of PBG waveguide results in very high quality structures as can be seen in Figure 7.

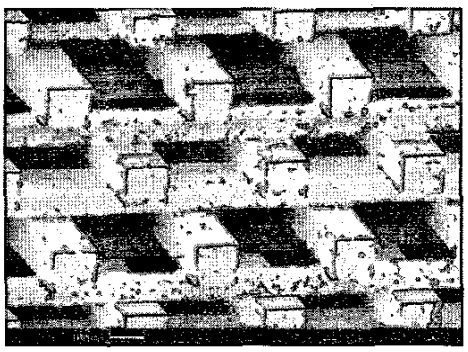

Figure 7: 250GHz PBG waveguide woodpile structures

The insertion loss of the waveguide will be measured in the near future but simulations in HFSS using realistic

values for the silicon resistivity (<1000 Ohms) predict them to be very low.

As well as the simple waveguide structures shown above more complicated structures such as couplers power splitters, horizontal and vertical bends were designed and part fabricated.

Silicon has been used as lens material for some time in the millimeter wave region. These however are difficult to make and hence expensive. In addition, its high refractive index requires a matching layer to prevent unnecessary reflection loss. By patterning and selectively removing silicon from the appropriate regions it is possible to realize flat optical elements such as the Fresnel lens using what is effectively and artificial dielectric. By using the high accuracy of the deep RIE etching process silicon structures can be realized with an effective permitivity of 1.5 or less. Using the material with the contrast of its natural properties all kinds of optics can be realized by stacking a number of suitably patterned layers on top of one another. As a proof of principle a Fresnel lens was designed and part fabricated using the deep RIE process. An image of one of the 7 layers is shown in Figure 8. Finished, the lens would be approximately 1mm thick and 15mm in diameter.

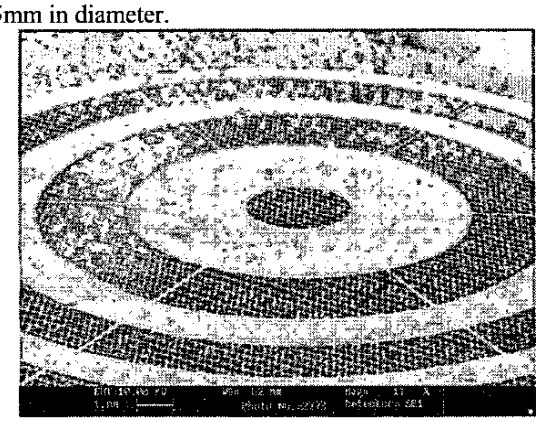

Figure 8: Silicon machined Fresnel lens

III. CONCLUSIONS

The use of deep RIE etching of silicon provides a new method for the manufacture of Terahertz RF circuitry. When combined with state of the art, full field design tools, complicated systems can be envisaged. All elements of the systems can be fabricated in this way including assembly aids and mechanical fixtures can also be realised in this manner along with the required optical elements.

PBG waveguide fabricated lithographically can provide a three dimensional circuit architecture where metalisation of the silicon is not required.

II. ACKNOWLEDGEMENTS

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